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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,902	02/13/2004	Kenneth Koch II	10017912-3	6091

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,902	KOCH ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17 and 22-27* is/are rejected.

7)☒ Claim(s) *18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 11/14/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patents 6,753,708 and 6,759,880 and U.S. application No. 10/777,174 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Specification

2. The substitute specification filed 11/14/05 has not been entered because it does not conform to 37 CFR 1.125(b) and (c) because: there is no accompanying statement that the substitute specification contains no new matter.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 4, 9, 11-13 and 25-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 3, the recitation "a DC power supply terminal" on line 2 is indefinite because it is not clear whether it is one of the "opposite power supply terminals" recited earlier (line 6, claim 1), or it is in addition to the opposite power supply terminals. Clarification and/or appropriate correction is requested.

Claim 4 is indefinite because it includes the indefiniteness of claim 3.

With respect to claim 7, the recitation "the power supply terminal" on line 4 lacks clear antecedent basis, and it is not clear if it is one of the "opposite power supply terminals" recited earlier (line 6, claim 1). Clarification and/or appropriate correction is requested.

With respect to claim 9, the recitation "first and second power supply terminal" on line 3 is indefinite because it is not clear if first and second power supply terminals are for the "opposite power supply terminals" recited earlier (line 6, claim 1), or they are in addition to the "opposite power supply terminals". Clarification and/or appropriate correction is requested.

Claims 11-13 and 25 are indefinite because they include the indefiniteness of claim 9.

Also, in claim 25, "positive power supply terminal" and "negative power supply terminal" recited in this claim are indefinite because it is not clear if they are the same as the first and second power supply terminals recited earlier in claim 9, and whether they are the opposite power supply terminals (claim 1) or they are in addition to the opposite power supply terminals. Clarification and/or appropriate correction is requested.

With respect to claim 26, the recitation "to the input terminals to each other and the thresholds being such that in response to" on lines 16-17 is indefinite because "the input terminals" lacks antecedent basis, and "the thresholds" lacks clear antecedent basis since it is not clear which thresholds that it is referred to. Further, "to each other and the thresholds being such" in the above phrase is indefinite because it is not clear what it is exactly means (i.e. the thresholds being "what"?). Clarification and/or appropriate correction is requested.

Claim 27 is indefinite because it includes the indefiniteness of claim 26.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-9, 11-17 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui et al. (USP 6,201,752) in view of Wanlass (USP 3,356,858).

With respect to claim 1, Figure 8A discloses a circuit, which includes: a first terminal (801) for receiving a voltage source (IN); a driver (inverter 809); an output terminal (810); and circuitry (802, 803, 805, 806, 807, 808) including at least one switchable capacitor (807 or 808) connected as recited in claim 1. The Bui et al. reference does not disclose that the inverter 809 comprise a PMOS and an NMOS transistor. However, the Wanlass reference discloses in Figure 5 that a CMOS inverter is easily formed by using a PMOS transistor connected with an NMOS transistor, wherein the CMOS inverter provides advantage such as low power consumption. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 8A of Bui et al. by using CMOS inverter having a PMOS and an NMOS as taught in Figure 5 of Wanlass for the inverter 809 (Figure 8A, Bui et al.) for the purpose of reduce power consumption. Thus, this modification meets all the limitations of claim 1. Note that the circuit now including first (PMOS inside CMOS inverter 809) and second (NMOS inside CMOS inverter 809) opposite conductivity type transistors, each includes a control electrode (gate) and a path (drain-source path) switched on and off in response to the control electrode being on opposite sites of a threshold, the first and second paths being

connected in series across opposite power supply terminals (power voltage and ground of the circuitry). Note that the operation of the modification of Figure 8A also meets the functional limitations of the circuitry recited ion the last 9 lines of the claim because the PMOS transistor having opposite conductivity with the NMOS transistor, so when the PMOS transistor is ON then the NMOS transistor is OFF (see discussion in the Wanlass reference for the turn on/off of PMOS and NMOS transistor, line 55 of Col. 4 to line 41 of Col. 5). Also, note that the switchable capacitor 807 (formed by using a PMOS transistor) so it has a different threshold with the switchable capacitor 808 (formed by using an NMOS transistor). Also, because the structure of claim is fully met and is similar as applicant's claimed invention, so the functional limitations of the claims are also met (see In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977), and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

With respect to claim 4, Figure 8A in the above modification shows the circuitry including at least one resistive element (either 803 or 805).

With respect to claim 5, the above modification shows the first and second transistors (PMOS and NMOS inside of inverter 809) are respectively a PFET and an NFET, and the at least one switchable capacitor (807) including a PFET having a first electrode (gate) connected to a gate electrode of the NFET transistor (NMOS inside inverter 809) of the driver and a second electrode connected to power supply.

With respect to claim 6, Figure 8A shows the resistive element (803 or 805) comprises a resistor, and the PFET and NFET of the driver, and the at least one switchable capacitor are included on an integrated circuit chip.

With respect to claim 7, the above modification of Figure 8A shows the first and second transistors (PMOS and NMOS inside of inverter 809) are respectively a PFET and an NFET, and the at least one switchable capacitor (808) including an NFET having a first electrode (gate) connected to a gate electrode of the PFET transistor (NMOS inside inverter 809) of the driver and a second electrode connected to ground.

With respect to claim 8, the above modification of Figure 8A shows the at least one switchable capacitor (807, 808) includes a first switchable capacitor (808) and a second switchable capacitor (807) respectively connected to the control electrodes of the first (PMOS transistor inside 809) and second (NMOS transistor inside 809) transistors.

With respect to claims 9 and 25, the above modification of Figure 8A shows the first and second capacitors (808 and 807) respectively connected between the control electrodes of the first and second transistors (PMOS and NMOS inside of 809), first and second power supply terminals (ground and power supply), and the first and second capacitors (NMOS 808 and PMOS 807). Note the functional recitation regarding finite capacitance and open circuit recited on the last 5 lines of the claim is inherently met because the structures of the first and second capacitors (transistor connected capacitor) are similar as applicant's invention. Note that the first and second threshold voltages of the first and second capacitors, respectively, are different because the threshold for PMOS transistor is different from the threshold voltage for NMOS transistor.

With respect to claim 11, Figure 8 shows the circuitry including first and second resistive elements (805 and 803).

With respect to claim 12, Figure 8A shows the first and second transistors (PMOS and NMOS inside 809) are PFET and NFET (inside 809) and the first and second capacitors (808 and 807) are respectively an NFET (808) and a PFET (807).

With respect to claim 13, Figure 8A shows the first and second transistors, the first and second capacitors and the first and second resistive elements are included in an integrated circuit chip.

With respect to claim 14, Figure 8A shows the circuitry including a first inverter (802-803, because when input IN = Lo then 802-803 output a Hi, which is reasonable to be considered as an inverter), and a second inverter (805-806, because when input IN = Hi then 805-806 outputs a Lo which is also reasonable to be considered as an inverter) each having an input terminal (at the gate of 802 for the first inverter, and at the gate of 806 for the second inverter), an output terminal (at the end of resistor 803 that connected to terminal 804 for the first inverter, and at the end of resistor 805 that also connected to terminal 804 for the second inverter), a first DC path (path through resistor 803) and a second DC path (path through resistor 805).

With respect to claim 15, Figure 8A shows the first and second transistors (PMOS and NMOS inside 809) are field effect transistors, the first and second inverters (802-803 and 805-806) comprise field effect transistors (802 and 806), and the first and second capacitors (808, 807) comprise field effect transistors.

With respect to claims 16-17, Figure 8A shows all the transistors are included on an integrated circuit chip, and including first and second resistors (803, 805) of the respective first and second inverters.

With respect to claims 22-24, Figure 8A shows a circuit including first and second opposite conductivity transistors (PMOS and NMOS transistors inside 809), opposite first and second power supply terminals (power voltage and ground), an output terminal (810), and first and second switchable capacitors (808 and 807) with the connections that meets all the structural limitations as discussed above with regard to the apparatus claims. Hence, the operation of Figure 8A meets all the method steps recited in claims 22-24.

With respect to claim 26-27, the modification as discussed in claim 1 above also meets all the limitations of these claims. Note that the driver includes first and second opposite conductivity type of transistors (PMOS and NMOS transistors in inverter 809), input terminal (IN) first and second opposite power supply terminals (positive power and ground) a first switchable capacitor (NMOS 808) connected between the control terminal (gate) of first transistor (PMOS) and the second power supply terminal (ground), a second switchable capacitor (PMOS 807) connected between the control terminal (gate) of second transistor (NMOS) and the first power supply terminal (positive power supply). Note that the first and second transistor (PMOS and NMOS inside inverter 809) having respective first and second thresholds (every transistor must have a threshold voltage), and the first and second switchable capacitors (NMOS 808 and PMOS 807) having third and fourth thresholds (every transistor must have a threshold voltage). Note that, because the structure of claim is fully met and is similar as applicant's claimed invention, so the functional limitations of the claims are also met (see In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977), and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Allowable Subject Matter

7. Claims 18-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the indefiniteness and informalities set forth above.

Responses to Arguments

8. Applicant's arguments filed on 11/14/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 23, 2006

LONG NGUYEN
PRIMARY EXAMINER